REMARKS

Reconsideration of the application in view of the above amendments and the following remarks is requested. Claims 16-35 are in this application. Claims 1-15 have been cancelled. Claims 16 and 18 have been amended. Claims 20-35 have been added to alternately and additionally claim the present invention.

The Examiner required that the invention be restricted to claims 1-15 or claims 16-19, which are drawn to a method of forming an imager. Applicant hereby affirms an election to prosecute claims 16-19.

The Examiner rejected claim 16 under 35 U.S.C. §102(b) as being anticipated by Hynecek (U.S. Patent No. 5,151,380). For the reasons set forth below, applicant respectfully traverses this rejection as applied to amended claim 16.

Amended claim 16 recites, in part:

> "forming a layer of isolation material on the second semiconductor region;
>
> "forming a layer of metal over the layer of isolation material over the second semiconductor region; and
>
> "etching the layer of metal to form a plurality of openings in the layer of metal, the plurality of openings including a first opening that vertically lies over a first pn junction region, a second opening that vertically lies over a second pn junction region, and a third opening that vertically lies over a third pn junction region, the layer of metal being electrically isolated from the first and second semiconductor regions."

In rejecting claim 16, the Examiner appears to point to p-type substrate 20 shown in FIG. 2D of Hynecek as constituting the first semiconductor region, and n-type regions 34 shown in FIG. 2D of Hynecek as constituting the second semiconductor region which has first, second, and third pn junctions. In addition, the Examiner appears to point to aluminum contact metal layer 32 as constituting

the layer of metal required by claim 16, and to the openings that lie between the final top bus structure 32 as constituting the plurality of openings.

However, metal layer 32/bus structure 32 can not be read to be the layer of metal required by claim 16 because the layer of metal must be electrically isolated from the first and second semiconductor regions. As taught by the Hynecek reference, the "top bus 32 makes contact with the substrate 20." (See column 5, lines 21-23 of Hynecek.)

As a result, it is not possible for metal layer 32/bus structure 32 to be electrically isolated from the first and second semiconductor regions. Thus, since the Hynecek reference fails to teach that metal layer 32/bus structure 32 is electrically isolated from the first and second semiconductor regions, claim 16 is not anticipated by the Hynecek reference. In addition, since claims 17 and 20-24 depend either directly or indirectly from claim 16, claims 17 and 20-24 are not anticipated by Hynecek for the same reasons as claim 16.

The Examiner objected to claims 18-19, but indicated that these claims would be allowable if amended to be in independent form including all of the limitations of the base claim and any intervening claims. (The Examiner originally indicated that claims 17-19 were objected to, but in a telephone call on or about July 6, 2004, the Examiner indicated that 17 was a typographical error and that claims 18-19 were objected to.) Claim 18 has been amended to be independent format, and is believed to include all of the limitations of independent claim 16. Claim 19 has not been amended to be in independent form as claim 19 depends from claim 18. In addition, new claims 25-29 depend either directly or indirectly from claim 18, and are thus patentable for the same reasons as claim 18.

New claim 30 recites, in part,

> "forming a layer of metal over the layer of insulation material; and
> "etching the layer of metal to form a plurality of spaced-apart openings in the layer of metal that lie over the plurality of second semiconductor regions, the layer of metal lying between two adjacent openings being electrically isolated from the second semiconductor regions that lie below the two adjacent openings."

However, as shown in FIG. 2D of Hynecek, metal structure 32 is electrically connected to the p+ region directly below it which, in turn, is electrically connected to the p+ regions that lie below the openings that lie on both sides of metal structure 32. Thus, it is not possible for the layer of metal that lies between two adjacent openings to be electrically isolated from the second semiconductor regions that lie below the two adjacent openings. As a result, new claim 30 is patentable over the Hynecek reference. In addition, since new claims 31-35 depend either directly or indirectly from new claim 30, new claims 31-35 are patentable over Hynecek for the same reasons as claim 30.

Thus, for the foregoing reasons, it is submitted that all of the claims are in a condition for allowance. Therefore, the Examiner's early re-examination and reconsideration are requested.

Respectfully submitted,

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